

Performing DCIR Measurements with a NOVONIX UHPC System

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Originally Published: 30-Nov-2023
Last Revised: 30-Nov-2023
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Introduction

The internal resistance of a battery can determine how it performs under load, in terms of how much capacity and energy can be delivered during a high-rate discharge. A battery is not an ohmic device, and therefore connecting a simple multimeter across the terminals will not produce a meaningful measure of the internal resistance. AC impedance measurements can be performed to understand the frequency response of the cell, and particular time constant or frequency ranges can be used to understand the role and limitations of individual cell components or interfaces. In this regard, AC impedance spectroscopy measurements are an excellent diagnostic probe into the functioning of a cell, but typical measurement frequencies are considerably higher than the DC limit where most constant-current cycling protocols operate. The DC response of a cell under a constant current may not be inferable from the AC response.

A proxy for the internal resistance of a cell can be obtained from a conventional constant-current cycling protocol without any special programming or additional measurements. The difference between the average charge and discharge voltage, often denoted as ΔV , represents twice the average polarization voltage change, referenced to the open-circuit voltage curve, over an entire cycle. The average polarization voltage change increases as the applied current increases. Assuming an ohmic response to the applied current, a measure of the average internal resistance can be related to ΔV according to

$$R_{\Delta V} = \frac{\Delta V}{2I} \quad (1)$$

where I is the applied current and $R_{\Delta V}$ is a measure of the average internal resistance derived from a ΔV measurement. ΔV is very useful for coarsely monitoring the internal resistance over the duration of a cycling experiment, but a major limitation is that it does not provide details of how the internal resistance varies across the entire voltage range or state-of-charge (SOC) swing within a cycle.

Obtaining the internal resistance as a function of state-of-charge can explain how a cell is aging and guide the programming of usage schemes in devices or applications. Typically, this is achieved by measuring the voltage response to a brief current pulse, applied at regular intervals throughout the discharge step of a particular cycle. These intervals are normally defined by a selected SOC change. It should be clear that the application of current pulses is a deviation of the test protocol from continuous constant-current cycling. From the voltage response to these DC current pulses, a resistance can be extracted, which is referred to as the DC internal resistance, DCIR, or R_{DC} . The values obtained for DCIR are dependent on the nature of the protocol used and the analysis methods applied to the voltage

response. As such, DCIR is not universal quantity, but utilizing a consistent method allows for relative comparisons to be made with more detail than can be obtained by measuring only ΔV . The measurement of DCIR can also be incorporated in a long duration cycling protocol, as it does not require the transfer of cells to separate, specialized hardware or integrated hardware with a battery cycler, such as would be required for EIS measurements. An example of this would be a cycling protocol that uses 1C charge and discharge currents, but every 100 cycles, the DCIR, low-rate capacity and other performance metrics could be measured before 1C cycling is resumed.

Theory

The DC internal resistance is obtained by measuring the voltage response to an applied DC current. The applied current cause a polarization voltage change, where the measured cell voltage drops during discharge and increases during charge. The application of a current will cause the cell voltage to change due to both polarization and charging or discharging the cell to a slightly different SOC. The latter is due to the nature of the cell voltage-capacity curve, or simply the fact that the cell voltage varies as a function of SOC and applying current will cause the SOC to change. Values obtained for the DCIR should ideally exclude the contribution of changing SOC during data analysis.

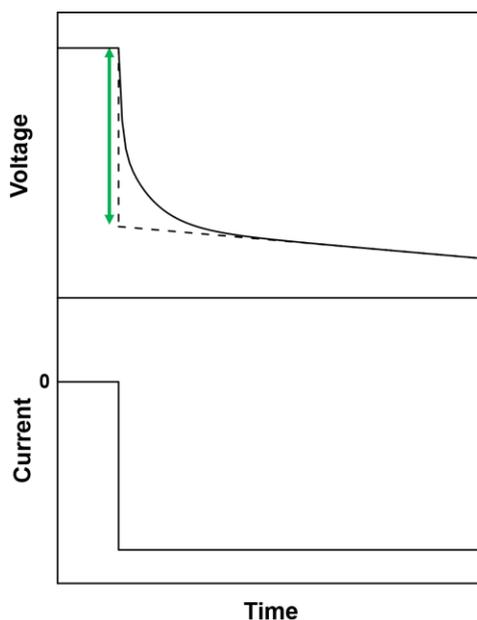


Figure 1. Idealized voltage and current versus time profiles for a battery subjected to a discharge current pulse. The end of the pulse is not shown here. Dashed lines indicate the projection of the linear, diffusion limited voltage regime back to the time at which the current pulse originates. The green arrow indicates the voltage drop which can be used to make a simple DCIR estimate, via Ohm's Law.

Figure 1 shows the idealized case of how the cell voltage responds during the application of a current pulse with constant magnitude (e.g., a rectangular pulse). When the current is switched on, the cell is polarized but quickly transitions to a linear decrease with increasing time. Over a short timescale or equivalently a narrow SOC range, the local shape of the cell voltage-capacity is approximately linear. The

linear voltage change shown in Figure 1 is ideally due exclusively to the variation of SOC as the cell is discharged, via processes that are diffusion limited, by which time the polarization effects are overcome. Subtracting the contributions of diffusion, or the SOC change, from the voltage data when the pulse starts yields just the effect of the polarization voltage drop, V_{drop} . This quantity, V_{drop} , is denoted by the green arrow in Figure 1. From this voltage drop, the resistance associated with that pulse can be computed from Ohm's Law, as per Equation 2.

$$R_{DC} = \frac{V_{drop}}{I} \quad (2)$$

Methods

DCIR measurements are dependent on both the protocol and analysis methods that are implemented. Standardized test methods include IEC 61690 and ISO 12405, but researchers often implement customized protocols that suit their cells and desired level of detail. In terms of hardware requirements, the measurement of DCIR benefits from battery cyclers with excellent current and voltage precision and accuracy, a wide current range to suit many cell sizes and probe them with a selection of currents and fast time resolution to track the fine details of voltage changes. NOVONIX Ultra-High Precision Coulometry (UHPC) products offer excellent measurement quality in terms of current and voltage, with a wide selection of current ranges available, with up to 20 A of maximum current. The maximum measurement frequency of a NOVONIX UHPC system is approximately 6 Hz, which allows for excellent voltage and current measurement quality, but does not yield high time resolution. As such, they are not well suited for the fast voltage tracking required for the most detailed DCIR measurements. Nevertheless, the system can accommodate simplified procedures that still provide excellent insight into cell kinetics and deliver relative performance comparisons.

In this example, Samsung 50E 21700 cylindrical cells (nominally 4.9 Ah) are used with a 10 A NOVONIX UHPC System and a NOVONIX 8-position thermal chamber. The thermal chamber was set to 25.0°C. The protocol file can be found on the NOVONIX website, hosted alongside this document, but a full text explanation follows here. The implementation of this protocol requires the usage of user-programmable variables and expressions to measure and portion the full discharge capacity into 10% SOC intervals. The reader is directed to the documentation "[UHPC Protocol – Getting started with custom variables and expressions](#)" for a prerequisite understanding of the implementation of variables and expressions in NOVONIX UHPC software. The required functionality is implemented in UHPC Protocol version 2.6.0 and Control version 2.7.0, or newer.

Figure 2 shows the sequence of steps used in this example, as programmed in UHPC Protocol. The protocol is explained as follows:

- The cell is charged to 4.2 V, the manufacturer specified upper cutoff voltage, at a rate of C/10, based on the nominal capacity.
- The cell is then discharged to 2.8 V at a rate of C/10. The capacity of this step is stored in a variable *var01* which represents 100% SOC.
- The cell is again charged to 4.2 V at a rate of C/10.
- The cell rests at open circuit for 15 minutes, before a 1C current is applied for 30 s, or until the cell voltage drops below 2.8 V. The latter end condition ensures cells are not over-discharged. The capacity of this 1C discharge is stored in a variable *var02*.
- The 1C discharge is followed by a C/5 discharge which is intended to discharge the cell to the next SOC interval. In this case, 1C pulses are applied every 10% SOC. The capacity of the 1C pulse (stored in *var02*) plus the capacity of the C/5 discharge should therefore be equal to 10% SOC. The capacity corresponding to 100% SOC is stored in *var01*, therefore the end condition for the C/5 discharge can be set to a step capacity equal to $var01/10 - var02$.
- Prior to the application of the next 1C pulse, the cell is again left at open circuit for 15 minutes.
- The process of applying a 1C pulse followed by a C/5 discharge is repeated 10 times, which should bring the cell to the fully discharged state.

Idea

Implement a DCIR measurement as part of a larger testing protocol. This could be before and/or after a conventional UHPC experiment, or collected at regular intervals (e.g., every 50 cycles) during a longer testing protocol.

Typical UHPC experiments range from a few weeks to more than a month. Only one or two additional days of testing are required to perform complementary DCIR measurements.

Protocol Control Step(s) + Reset Step Limits 

1	⋮ CC-CV Charge	10	C/xx ▾	to	4.2 V
2	⋮ Constant Current Discharge	10	C/xx ▾	to	2.8 V
3	⋮ Increment Cycle Counter				
4	⋮ CC-CV Charge	10	C/xx ▾	to	4.2 V
5	⋮ Open Circuit Storage				
↵ 6	⋮ Repeat steps below	10			times
7	⋮ Constant Current Discharge	1	C/xx ▾	to	2.8 V
8	⋮ Constant Current Discharge	5	C/xx ▾	to	2.8 V
9	⋮ Open Circuit Storage				

Figure 2. Screenshot of NOVONIX Protocol step list for performing DCIR measurements. Detailed screenshots of the step condition programming can be found in the Appendix at the end of this document.

Caution

In situations of higher kinetic stress, such as high pulse current, low temperature and cells with poor power capability, the voltage may drop more than expected during a discharge, causing the lower cutoff voltage of the step to trip and terminate the step before the pulse is complete.

Possible adjustments include:

- Using a lower pulse current
- Decreasing the lower cutoff voltage for the pulse (e.g., Step 7 in Figure 2) and adding a brief Open Circuit Storage step before the C/5 discharge (e.g., Step 8 in Figure 2)

The DCIR protocol discussed here can be summarized as a first cycle, to capture the full discharge capacity, which is used to define SOC increments, followed by a second cycle where the discharge is segmented into 10% SOC increments, with a rest, 1C pulse and C/5 discharge applied during each increment. This could be achieved with only a single cycle if the 100% SOC measurement is based on the charge capacity of the same cycle in which the 1C discharge pulses are applied, rather than the discharge capacity of a preceding cycle. Despite this, measuring SOC during a discharge is more accurate for how it is used during a DCIR protocol, hence the protocol design choices made here. A full series of screenshots displaying the protocol in greater detail can be found in the Appendix at the end of this document.

💡 Idea

The programmed pulse currents can be tailored to the cell size/capacity, along with system availability.

Pulsing with 1C can provide a large voltage change but may also result in larger SOC changes during the pulse than smaller currents. Smaller currents can provide equally meaningful results as larger currents. As long as there is a sufficient voltage response, the choice of current should not significantly affect the results, because current is not included in the final result, as shown in Equation 2.

Adjusting the pulse current can also extend the usage of a lower current system to cells with greater capacity. For instance, with a 5 Ah 21700 cylindrical cell, running a DCIR protocol *exactly* like the one proposed here would require a maximum current of 5 A to provide the 1C pulses. This would require a NOVONIX 10A or 20A UHPC System.

If the pulse current is decreased to $C/3$, the required current is only 1.67 A. This can be supplied by a NOVONIX 2A UHPC System, and enable DCIR measurements on such a cell in the event that a customer does not have 10A or 20A channels.

Analysis

At the time of writing, there is no means of extracting an effective resistance from DCIR experiments in NOVONIX UHPC Plot. This is largely because DCIR protocols are not universal, and the obtained results can depend on both the testing and analysis methods. Figure 3 shows the voltage versus time as displayed in UHPC Plot and gives a visual overview of the charging profile described in the previous section. The capacity which defines 100% SOC is measured during the discharge from $t = 10$ h to 20 h, and the resistance values are obtained from analyzing the 1C pulse data from the following discharge.

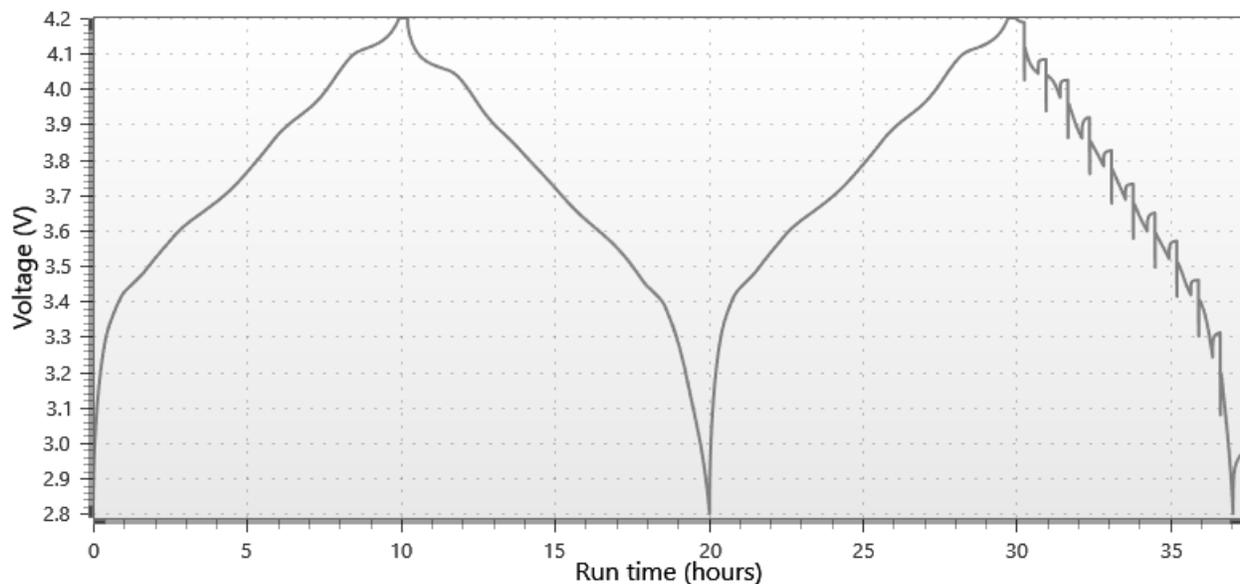


Figure 3. Voltage versus time, as shown in NOVONIX UHPC Plot, for a Samsung 50E 21700 cell undergoing the DCIR measurement protocol described herein.

Further analysis requires direct handling of the data, via a means that the user is comfortable with. This could include Microsoft Excel, Python, Mathworks MATLAB, etc. NOVONIX UHPC data is written as simple CSV files, with a header and labelled data columns, making accessing and parsing the data straightforward and convenient. Provided along side this document, hosted on the NOVONIX website, is python code, in the form of a Jupyter Notebook, which can perform the analysis described here or guide the reader in developing an analysis of their own. The provided code uses a few dependencies that may require installation depending on the package manager and distribution of Python used. The code blocks are well commented and therefore should be straightforward to understand.

The data is parsed, then the capacity of the first discharge is determined. This capacity is used to determine the current that corresponds to 1C. The rows of data in second discharge for which the current is close to 1C are then selected and divided into groups based on the step number. Figure 4 shows the voltage versus step time of the ten 1C discharge pulses, along with linear fits to the final ~25% of each profile. These fits, intended to capture the rate of voltage change during the diffusion limited regime of the pulse, are projected back to $t = 0$ h. Figure 4 shows an insufficient amount of data at the beginning of each pulse, yielding non-smooth evolution of the voltage profile at during the first few seconds and data points. The data collection intervals during the 1C pulses were set at 5 mV of voltage change and a 1 s time increment. Time increments of a few milliseconds would be ideal but are below the timing capabilities of a NOVONIX UHPC System. Nevertheless, the simple analysis performed here does not require a high degree of time resolution.

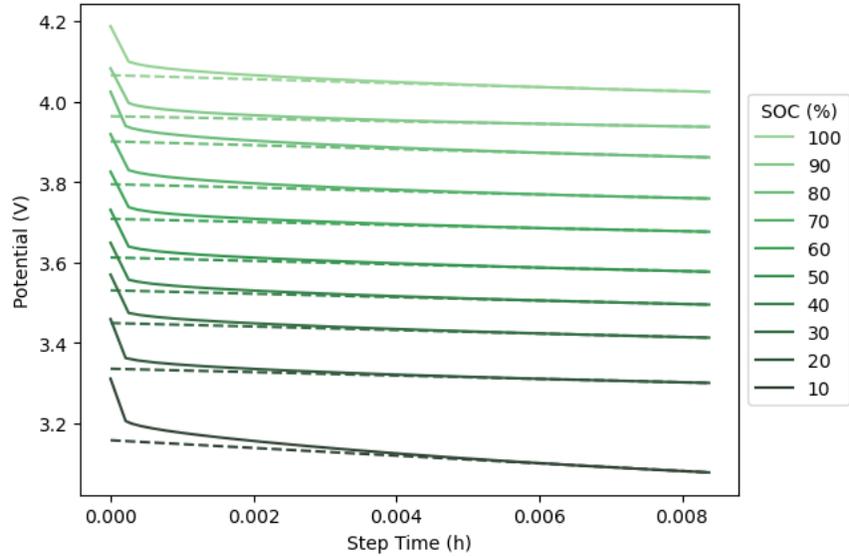


Figure 4. Voltage versus time profile for a Samsung 50E cell, during ten 1C pulses from which resistances can be extracted. Dashed lines indicate a linear fit to the final section of each profile, which is projected back to $t = 0$ h.

The value of the linear fit to the voltage vs time data, when $t = 0$ h, is subtracted from the measured voltage at $t = 0$ h, defining a voltage drop that can be entered into Equation 2. Figure 5 shows the calculated DC internal resistances as a function of state-of-charge. The shape is approximately concave, which is expected as cell impedance tends to increase at endpoint states of charge. This is due to the relative concentrations of charge carriers (Li atoms) and vacancies in each electrode at 0% and 100% causing behavior that tends towards blocking electrodes. If the total geometric area of the positive electrode is known, it would be excellent practice to represent the resistance in Figure 5 as an area specific resistance to facilitate a better comparison between cells of different sizes and constructions.

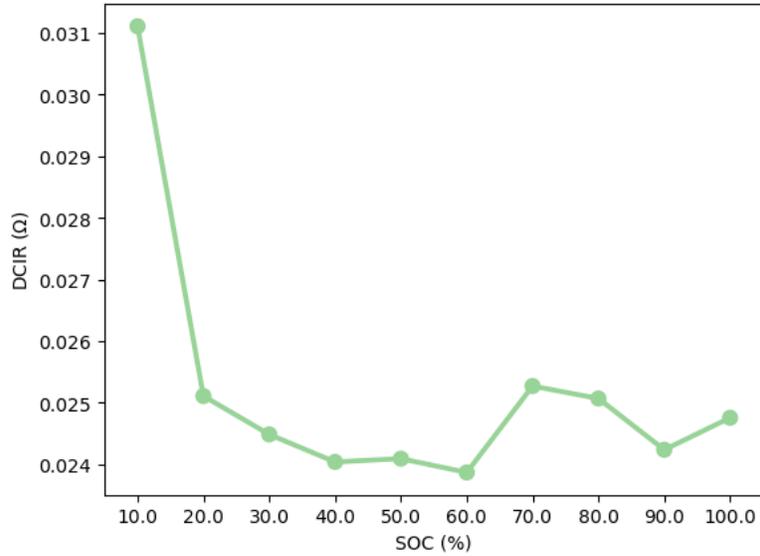


Figure 5. Resistance of a Samsung 50E 21700 cell, obtained from the DCIR method described herein, plotted as a function of state-of-charge.

Conclusions

Implementing DCIR measurements can enhance the utility of a NOVONIX UHPC System. This can provide kinetic information that is not typically available from conventional forms of UHPC cycling. This can guide usage schemes, such as setting SOC intervals for fast charge protocols, or provide more robust information to guide cell design or predictive modeling and lifetime projections. Being able to perform DCIR measurements sequentially with cycling experiments offers improved convenience and labor savings, where DCIR measurements might otherwise be made on another system, requiring manual intervention to relocate a cell and initiate new tests.

Appendix

The screenshot displays the 'Protocol Control Step(s)' and 'Step Control Conditions' panels. The 'Protocol Control Step(s)' panel shows a list of steps: 1: CC-CV Charge (10 C/xx to 4.2 V), 2: Constant Current Discharge (10 C/xx to 2.8 V), 3: Increment Cycle Counter, 4: CC-CV Charge (10 C/xx to 4.2 V), 5: Open Circuit Storage, 6: Repeat steps below 10 times, 7: Constant Current Discharge (1 C/xx to 2.8 V), 8: Constant Current Discharge (5 C/xx to 2.8 V), and 9: Open Circuit Storage. The 'Step Control Conditions' panel is for 'CC-CV Charge' (10 C/xx to 4.2 V). The 'Action' section includes 'End step' (Any time), 'Save data' (During CC), and 'Update Variable' (During CV). The 'When' section includes conditions: 'step time' (15 hours), 'abs()' (50 C/xx), 'ΔV' (0.005 V), 'Δt' (300 seconds), 'ΔI' (10 mA), and 'Δt' (300 seconds).

Figure A1. Screenshot of NOVONIX UHPC Protocol, showing the step control conditions for the C/10 constant-current constant-voltage charge implemented in steps 1 and 5 of the DCIR protocol described herein.

The screenshot displays the 'Protocol Control Step(s)' and 'Step Control Conditions' panels. The 'Protocol Control Step(s)' panel shows a list of steps: 1: CC-CV Charge (10 C/xx to 4.2 V), 2: Constant Current Discharge (10 C/xx to 2.8 V), 3: Increment Cycle Counter, 4: CC-CV Charge (10 C/xx to 4.2 V), 5: Open Circuit Storage, 6: Repeat steps below 10 times, 7: Constant Current Discharge (1 C/xx to 2.8 V), 8: Constant Current Discharge (5 C/xx to 2.8 V), and 9: Open Circuit Storage. The 'Step Control Conditions' panel is for 'Constant Current Discharge' (10 C/xx to 2.8 V). The 'Action' section includes 'End step' (Any time), 'Save data' (During CC), and 'Update Variable' (During CV). The 'When' section includes conditions: 'step time' (15 hours), 'ΔV' (0.005 V), 'Δt' (300 seconds), and 'Step Capacity' (var01 Ah).

Figure A2. Screenshot of NOVONIX UHPC Protocol, showing the step control conditions for the C/10 constant-current discharge implemented in step 2 of the DCIR protocol described herein.

The screenshot displays the 'Protocol Control Step(s)' and 'Step Control Conditions' panels. The 'Protocol Control Step(s)' panel shows a list of steps: 1: CC-CV Charge (10 C/xx to 4.2 V), 2: Constant Current Discharge (10 C/xx to 2.8 V), 3: Increment Cycle Counter, 4: CC-CV Charge (10 C/xx to 4.2 V), 5: Open Circuit Storage, 6: Repeat steps below 10 times, 7: Constant Current Discharge (1 C/xx to 2.8 V), 8: Constant Current Discharge (5 C/xx to 2.8 V), and 9: Open Circuit Storage. The 'Step Control Conditions' panel is for 'Open Circuit Storage'. The 'Action' section includes 'End step' (Any time), 'Save data' (During CC), and 'Update Variable' (During CV). The 'When' section includes conditions: 'step time' (15 minutes), 'ΔV' (0.005 V), and 'Δt' (1 seconds).

Figure A3. Screenshot of NOVONIX UHPC Protocol, showing the step control conditions for the open circuit storage implemented in steps 3 and 9 of the DCIR protocol described herein.

Protocol Control Step(s) + Reset Step Limits

- CC-CV Charge 10 C/xx to 4.2 V
- Constant Current Discharge 10 C/xx to 2.8 V
- Increment Cycle Counter
- CC-CV Charge 10 C/xx to 4.2 V
- Open Circuit Storage
- Repeat steps below 10 times
- Constant Current Discharge 1 C/xx to 2.8 V**
- Constant Current Discharge 5 C/xx to 2.8 V
- Open Circuit Storage

Step Control Conditions

Constant Current Discharge 1 C/xx to 2.8 V

Action + **When**

- End step Or step time > 30 seconds
- Save data Or ΔV > 0.005 V
- Update Variable Or Step Capacity = var02 Ah

Figure A4. Screenshot of NOVONIX UHPC Protocol, showing the step control conditions for the 1C constant-current discharge implemented in step 7 of the DCIR protocol described herein.

Protocol Control Step(s) + Reset Step Limits

- CC-CV Charge 10 C/xx to 4.2 V
- Constant Current Discharge 10 C/xx to 2.8 V
- Increment Cycle Counter
- CC-CV Charge 10 C/xx to 4.2 V
- Open Circuit Storage
- Repeat steps below 10 times
- Constant Current Discharge 1 C/xx to 2.8 V
- Constant Current Discharge 5 C/xx to 2.8 V**
- Open Circuit Storage

Step Control Conditions

Constant Current Discharge 5 C/xx to 2.8 V

Action + **When**

- End step Or Step Capacity > (var01/10)-var02 Ah
- Save data Or ΔV > 0.005 V
- Update Variable Or Δt > 30 seconds

Figure A5. Screenshot of NOVONIX UHPC Protocol, showing the step control conditions for the C/5 constant-current discharge implemented in step 8 of the DCIR protocol described herein.